Listing of Claims

1. (Currently Amended) A digital embedded architecture, including a microcontroller and a memory device, suitable for reconfigurable computing in digital signal processing and comprising:

a processor, ~~structured to implement a Very Long Instruction Word elaboration mode by a general purpose hardwired computational logic, and~~

a ~~an additional~~ data elaboration channel comprising a reconfigurable function unit based on a pipelined array of reconfigurable data-path oriented ~~configurable look-up table based~~ cells, and ~~controlled by~~

a special purpose reconfigurable control unit operable to control which rows of the array of reconfigurable data-path oriented cells are activated, each row representing a stage of a customized pipeline, the special purpose reconfigurable control unit controlling activation of the rows in a dataflow fashion.

2. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 1, wherein said reconfigurable function unit includes ~~[[a]]~~ hardware-based Field Programmable Gate Array (FPGA) embedded devices.

3. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 1, wherein said ~~additional~~ data elaboration channel is tightly integrated in a processor core, receiving inputs from a register file and writing results on dedicated write back channels over the register file.

4. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 1, wherein said pipelined array of reconfigurable data-path oriented ~~configurable look-up table based~~ cells implements a configurable run-time with a variable latency data path ~~capable to emulate a potentially infinite number of~~ emulating virtual application specific function units.

5. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 4, wherein the architecture is based on three different and concurrent data elaboration flows, two of which feed each cycle by instruction fetch and one based on an independent, variable latency pipeline implemented on the reconfigurable ~~configurable~~ data-path.

6. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 2, wherein said ~~configurable~~ gate-array is ~~a Pipelined Configurable Array (PiCo Array) comprising~~ a pipelined array of configurable lookup-table based cells virtually emulating a microprocessor data path.

7. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 1 ~~[[6]]~~, ~~wherein the cells of said PiCo-Array structure are grouped in rows, each representing a possible stage of a customized pipeline, and~~ the whole array being ~~can be~~ represented by a control data flow graph, each row or group of rows corresponding to a different state and being controlled for activation by the special purpose reconfigurable control unit.

8. (Canceled).

9. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 1 ~~[[3]]~~, wherein said special purpose reconfigurable control unit is a hardwired, run-time programmable Data-Flow-Graph based control unit synchronizing ~~the~~ pipelined computation by ~~of~~ the gate-array cells.

10. (Canceled).

11. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 3, wherein said register file comprises four read ports, used to support the issue of two RISC instructions each clock cycle, and two write ports reserved for said two hardwired pipeline channels; two other ports being entirely dedicated to write back results of the pipelined array, thus avoiding introduction of dedicated logic handling competition on the register file ports.

12. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 1, wherein said pipelined array comprises a first level cache, storing four configurations for each logic cell; and further comprising a context switch for taking only one clock cycle and providing four immediately available instructions.

13. (Canceled).

14. (Currently Amended) The ~~[[A]]~~ digital embedded architecture according to claim 1, further comprising a ~~special purpose~~ reconfiguration mechanism for allowing very fast configuration completely concurrent with processor execution, said reconfiguration mechanism including the configurable array being structured in blocks, having at least eight rows each, each block being reprogrammed while the other blocks are under execution.

Claims 15-25. (Canceled).

26. (New) The digital embedded architecture according to claim 1, wherein the control unit is further operable to control synchronization of the array of reconfigurable data-path oriented cells and the processor.

27. (New) The digital embedded architecture according to claim 1, wherein the rows are grouped together to form a pipeline stage of an implemented data-path.

28. (New) The digital embedded architecture according to claim 27, wherein the control unit controls pipeline execution of the array of reconfigurable data-path oriented cells by using a dataflow model to calculate for each cycle which row is to perform computations.

29. (New) The digital embedded architecture according to claim 27, wherein the control unit generates control signals for each row selectively activating the rows of the pipeline stages to make computations in each clock cycle.

30. (New) The digital embedded architecture according to claim 27, wherein the cells of the array generate signals to cause the control unit to implement data-dependent conditional executions.

31. (New) The digital embedded architecture according to claim 27, wherein the pipelined array of reconfigurable data-path oriented cells implements a configurable run-time with a variable latency data path with each row being controlled by control signals generated by the control unit so as to be capable of emulating virtual application specific function units.

32. (New) The digital embedded architecture according to claim 27, wherein the data elaboration channel is tightly integrated in a processor core receiving inputs from a register file and writing results on dedicated write back channels over the register file, and further is linked with the processor core through an interface between processor control logic and the control unit.

33. (New) The digital embedded architecture according to claim 32, wherein a destination register file corresponding to any decoded instruction of the pipelined array is locked so as to cause a processor stall in response to any following decoded instruction which would also access that destination register file, and wherein normal execution is restored when the pipelined array completes a write-back operation and the destination register is unlocked.

34. (New) The digital embedded architecture according to claim 33, wherein the locking of the destination register file supports enhanced levels of resource utilization parallelism by allowing unpredictable latency instructions to be executed on the configurable unit without altering program flow consistency.

35. (New) The digital embedded architecture according to claim 1, wherein the array of reconfigurable data-path oriented cells and control unit are multi-context to provide a first level cache of immediately available functions by integrating in the array and control unit additional memory cells for each configuration bit.

36. (New) The digital embedded architecture according to claim 1, wherein the array of reconfigurable data-path oriented cells is organized in regions, each region being composed of a configurable number of array rows, and wherein a region is reprogrammed while other regions are under execution and the control unit controls operation of the cells in each region and controls operation between regions.

37. (New) The digital embedded architecture according to claim 36, wherein the regions compute in parallel, the regions being activated by the control unit for writeback operation.

38. (New) A digital embedded architecture, comprising:

an array of reconfigurable data-path oriented cells arranged in rows, each row representing a stage of a processing pipeline;

a configuration control unit operable to configure the array of reconfigurable data-path oriented cells; and

an operation control unit operable to control in a dataflow fashion which rows of the array of reconfigurable data-path oriented cells are activated to implement the processing pipeline.

39. (New) The digital embedded architecture of claim 38 wherein the operation control unit generates control signals each clock cycle which activate only those rows of the array that are involved in a computation phase to be executed in that clock cycle.